Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **Y1**
3. **A2**
4. **Y2**
5. **A3**
6. **Y3**
7. **GND**
8. **Y4**
9. **A4**
10. **Y5**
11. **A5**
12. **Y6**
13. **A6**
14. **VCC**

**.042”**

**1 14 13**

**12**

**11**

**10**

**9**

**8**

**6 7**

**2**

**3**

**4**

**5**

**MASK**

**REF**

**D**

**54C14**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC**

**Mask Ref: 54C14 D**

**APPROVED BY: DK DIE SIZE .042” X .065” DATE: 5/30/23**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54C14**

**DG 10.1.2**

#### Rev B, 7/1